Appl. No. 09/802,120
Amdt. dated July 21, 2004
Reply to Office Action of April 26, 2004

PATENT

Amendments to the Specification:

Please replace paragraph beginning on page 13, line 24, with the following amended paragraph:

On the other hand, by calculating a 64-bit address using the program counter, the number of instructions can be greatly reduced. For example, the following is a list of instructions which will calculate a 64-bit address using the program counter:

add R0, 1, Rx	(Add 1 to the value in R, (which is zero) and place the result in register Rx. The affect is that Rx holds the value 1.)
sll Rx, 20, Rx	(Logical left shift of the value in register Rx by 20 bits and place the results in register Rx. The affect is to change the value in register Rx, from ~~20~~ $\underline{2^0}$ or 1 to ~~220~~ $\underline{2^{20}}$ or 1,048,576.)
ld [Rpc + Rx], R	(Load the value stored in memory at address [Rpc + Rx]

into register R. The affect is to load register R with a value of a memory location which is offset from the program counter by ~~220~~ $\underline{2^{20}}$ or 1MB.)